CLAIMS

1. (**Amended**) A data processor comprising a first arithmetic and logic unit controlled by a CPU, first storage means, a local data bus having a bus width wider than a data bus width of said CPU and connecting **the** first arithmetic and logic unit and **the** first storage means, and an address bus commonly connected to said CPU, **the** first arithmetic and logic unit, and said first storage means.

2. The data processor according to claim 1, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIDM type.

3. The data processor according to claim 1, wherein a plurality of said first arithmetic and logic units are arranged in parallel.

4. The data processor according to claim 1, wherein said first storage means has a first memory, a second memory, and a DMA circuit connected to said address bus and said data bus and controlling data transfer between the first and second memories.

5. The data processor according to claim 4, wherein said first storage means has means for performing sign extension when data is transferred from said second memory to said first memory by the DMA

circuit.

6. The data processor according to claim 4, wherein said first memory has first and second work memories, and said first storage means further comprises means for alternately switching between connection of the first and second work memories to said first arithmetic and logic unit and said second memory, respectively, and connection of the first and second work memories to said second memory and said first arithmetic and logic unit, respectively.

7. The data processor according to claim 1, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIMD control type for parallelly performing arithmetic process on plural data by a single instruction from said CPU.

8. The data processor according to any one of claims 1 to 7, wherein said first arithmetic and logic unit taking the form of an SIMD control type arithmetic and logic unit, comprising: a plurality of processor elements each having a first input terminal, a second input terminal, and a first output terminal and operated by a control signal from said CPU; a first register having a bit width equal to a total of bit widths of input terminals of all of first input terminals of said plurality of processor elements; a

second register having a bit width equal to a total of bit widths of second input terminals of all of said plurality of processor elements and applying all the bit widths to the second input terminals of all the processor elements without an overlap; a third register having a bit width equal to or wider than a bit width of the second input terminal of each of said processor elements and capable of shifting data to the second register on a unit basis of the bit width of the second input terminal; a selector for selecting data of said first register and supplying the bit width of the first input terminal of said processor element from the most significant bit commonly to the first input terminals of all of said processor elements; a write control circuit controlled by said address bus, for writing data to said first, second, and third registers via said local bus; and a circuit for outputting data of said output terminal to said local data bus.

9. The data processor for image processing according to claim 8, wherein said processor element is an arithmetic and logic circuit for adding up a subtraction value of data of said first and second input terminals for a predetermined range and outputting resultant data, data is stored in a plurality of pixels of an image to be encoded in said first register, data of a plurality of pixels of a reference image to be referred to is stored in said

second register, and outputs of said plurality of processor elements are taken as the degree of approximation corresponding to a plurality of motion vectors.

10. An arithmetic and logic unit of an SIMD control type, comprising: a plurality of processor elements each having a first input terminal, a second input terminal, and a first output terminal; a first register having a bit width equal to a total of bit widths of first input terminals of all of said plurality of processor elements; a second register having a bit width equal to a total of bit widths of second input terminals of all of said processor elements; and a third register having a bit width equal to or wider than a bit width of the second input terminal of said processor element and capable of shifting data to the second register on a unit basis of the bit width of the second input terminal.

11. The SIMD control type arithmetic and logic unit according to claim 10, wherein said first register has a connection circuit for commonly supplying a bit width of a first input terminal of said processor element from the most significant bit to all of said processor elements, and a connection circuit for supplying all of bit widths so as not to be overlapped to all of the processor elements.

12. The SIMD control type arithmetic and logic unit according to claim 10, further comprising: a selector for supplying the bit width of the first input terminal of said processor element from the most significant bit of said first register to all of said processor elements; and means for performing, every clock, an arithmetic process in said processor element, a data shifting process on the unit basis of the bit width of the first input terminal of said processor element in said first register, and a data shifting process on the unit basis of the bit width of the second input terminal of said processor element in said second and third registers.

13. The SIMD control type arithmetic and logic unit according to claim 11 or 12, used for image processing, wherein data of a plurality of pixels in a first image is stored in said first register, data of a plurality of pixels in a second image is stored in said second and third registers, said processor element takes the form of an arithmetic and logic circuit for accumulating a difference between data applied from said first input terminal and data applied from said second input terminal, and means for outputting the degree of approximation corresponding to a plurality of motion vectors between said first and second images from each of said plurality of processor elements is

provided.

14. (**added**) A data processor having a CPU, a first arithmetic unit, storage means, an address bus connecting said CPU and said storage means and a local data bus connecting the first arithmetic unit and the storage means wherein said CPU comprises a instruction decode circuit decoding a instruction, output of which controls said first arithmetic unit, and said local data bus having a bus width wider than a data bus width.

15. (**added**) A data processor according to claim14, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIDM type.

16. (**added**) A data processor comprising;

a CPU, a first arithmetic and logic unit controlled by said CPU, storage means connected with said CPU by address bus, a DMA circuit connected with said address bus and said storage means, and

a local data bus having a bus width wider than a data bus width of said CPU and connecting the arithmetic and logic unit and the storage means.

17. (**added**) A data processor according to claim16, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIDM type.

18. (**added**) A data processor comprising;

a first storage means stored instructions, a CPU connected with said first storage means through an address bus and a first data bus, a second storage means connected with said CPU through said address bus, and

an arithmetic and logic unit connected with said second storage means through an second data bus having bus width wider than data bus width of said first data bus.

19 (**added**) A data processor according to claim18, wherein said arithmetic and logic unit is an arithmetic and logic unit of an SIDM type.

20. (**added**) A data processor according to claim18 or 19, which further comprises a DMA circuit connected to said address bus, said first data bus and said second memories.